THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte SHUHEI SUDO
and
MAKIO YAMAKI

_____

Appeal No. 95-4084
Application 07/992,648[1]

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HEARD: October 17, 1997

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Before HAIRSTON, BARRETT, and FLEMING, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

[1] Application for patent filed December 18, 1992.

This is an appeal from the final rejection of claims 1 and 2. In an Amendment After Final (paper number 14), claim 1 was amended.

The disclosed invention relates to a coefficient data change processing method for a digital signal processor of a pipeline system that has a coefficient address pointer independent of a program counter, and that transfers and supplies a processing program and coefficient data from a microprocessor during read cycle steal operating processes. According to appellants, the read cycle steal processes for transferring coefficient data are spread out across three machine stages (i.e., fetch, decode and execute), rather than the single stage (i.e., execute) of the prior art.

Claim 1 is the only independent claim on appeal, and it reads as follows:

1. A coefficient data change processing method for a digital signal processor of a pipeline system which has a coefficient address pointer independent of a program counter, and transfers and supplies a processing program and coefficient data from a microcomputer, said method comprising the steps of:

discriminating whether an instruction is a read instruction of said coefficient data at which a read cycle steal should be executed from a value of said program counter;

when said instruction is a read instruction, transferring new coefficient data during an instruction read stage and an instruction decode stage in a processing unit to a transfer buffer from said microcomputer; and

writing said coefficient data stored in said transfer buffer into a coefficient data memory by said read cycle steal at an execution stage in said processing unit.

The references relied on by the examiner are:

Garrett et al. (Garrett)	4,991,217	Feb. 5, 1991
Yamaki et al. (Yamaki)	5,218,710	June 8, 1993 (filed Jan. 22, 1990)

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as being unpatentable over Yamaki in view of Garrett.

Reference is made to the briefs and the answers for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection.

The examiner is of the opinion that Yamaki discloses the claimed method, but did not "specifically disclose the steps of discriminating whether an instruction is a read instruction or writing data into a coefficient data memory by said read cycle steal" (Answer, pages 3 and 4). For a teaching of the missing steps, the examiner turned to the dual processor speech recognition system teachings of Garrett. The examiner indicates (Answer, page 4) that:

> Garrett et al. disclosed the steps of discriminating whether an instruction is a read instruction from a value of said program counter (col. 19, line 30, et seq.) and writing data into a coefficient data memory

> by said read cycle steal (col. 28, line 19, et seq.). It would have been obvious to one of ordinary skill in the art at the time of Appellant's [sic] invention to incorporate Garrett et al.'s cycle steal sequencer into the Yamaki et al. system because Garrett et al.'s cycle steal sequencer would increase the throughput of the Yamaki et al. system by allowing for the transfer of coefficient data upon the detection of a read instruction.

Appellants acknowledge the structural similarities between the disclosed system and the system disclosed in Yamaki, but argue that the method by which the Yamaki system replaces coefficient data is very different from the method recited in the claims (Brief, page 9). Appellants also argue that "Yamaki fails to suggest a read cycle steal as recited in claim 1, or anything equivalent" (Brief, page 13), and that "Yamaki nowhere discloses scheduling different DSP functions during particular stages of the three machine cycles (read or fetch stage, decode stage, execute stage) used in pipeline processing" (Brief, page 14).

During the transfer of coefficient data (column 9, lines 18 through 63) in Figure 1 of Yamaki, the microcomputer supplies a muting control instruction to sequence controller 18 which then places the system in a muting condition via muting switch circuit 30. The microcomputer then reads a sequence control program, coefficient data, and other data corresponding to a newly selected sound field from ROM. The sequence control program is

transferred to program RAM 19, and the coefficient data is transferred to the transfer buffer 27. After transferring the coefficient data to the transfer buffer, the microcomputer issues a data change-over command and an initialization command to the sequence controller 18. In response to the data change-over command, the sequence controller 18 issues a predetermined instruction signal to the memory control circuit 34 to write the coefficient data group in the transfer buffer 27 into a predetermined area of the coefficient data RAM 10. The microcomputer thereafter cancels the muted condition, and the newly written coefficient data is read from the coefficient data RAM 10 to the buffer memory 7 to start the new sound field.

In view of the foregoing coefficient data transfer operation in Yamaki, we agree with appellants: that the method of transferring new coefficient data in Yamaki is completely different from the method of transferring new coefficient data in claim 1; that Yamaki is not concerned with read cycle steal; and that the claimed three stages of transferring new coefficient data to a coefficient data memory are not addressed by Yamaki.

We agree with the examiner (Answer, page 4) that Garrett discloses a cycle steal sequencer. Even if we assume for the sake of argument that the skilled artisan would have found it

obvious to modify Yamaki in light of the teachings of Garrett, we fail to see how Garrett's cycle steal sequencer "would increase the throughput of the Yamaki et al. system" (Answer, page 4) since Garrett halts the signal processor 63 "for no more than four machine cycles" (column 19, lines 24 through 28). The halting of the signal processor in Garrett coupled with Yamaki's muting of the sound would certainly decrease, as opposed to increase, the throughput of the Yamaki system. Thus, we agree with appellants that "the cycle steal sequencer of Garrett fails to satisfy the 'read cycle steal' feature of claim 1, which, by definition, operates without interrupting production of DSP output signals" (Reply Brief, pages 5 and 6). The obviousness rejection of claims 1 and 2 is reversed.

DECISION

The decision of the examiner rejecting claims 1 and 2 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)

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